David Bulos

Website | Email | LinkedIn | Phone

Education

Electrical & Computer Engineering Undergraduate — London, ON, Canada
University of Western Ontario — *2023 – 2028*

- Maintaining an 86.8% average; awarded Dean's Honor List recognition for consecutive years.
- Excelled in core courses: Circuits & Systems (98%), Applied Math II (99%), Digital Logic (95%), & Electric Circuits (93%).

Technical Skills

Programming: C++, Python, Java, MATLAB/Simulink, Linux, PlatformIO
Electrical Design: Altium, Cadence Allegro PCB Editor, Sigrity SI/PI (SigXp, PowerDC, SystemSI), SPICE Simulations, MCU Integration, Quartus, AutoCAD Electrical, Serial Communication (CAN, UART, IsoSPI, I2C), CANKing

Experience

Ciena | Optical Networking — Ottawa, ON
Modem Hardware Intern — *Sept 2025 – Apr 2026*

- Developing Python test scripts via Paramiko and TCP clients to execute IRIS ASIC boundary scans and bump qualification, streamlining validation testing hand-offs to manufacturing partners like Sanmina.
- Characterizing precision DACs and power regulators using ADI ACE software and DC electronic loads to validate efficiency, VMON/IMON accuracy, and voltage headroom/footroom against datasheet specifications.
- Validating high-speed signal integrity by selecting optimal IBIS models in Sigrity, correlating simulations with benchtop TDR and phase noise measurements using Vector Network and Spectrum Analyzers.
- Isolating faults on pluggable optical modems by cross-referencing schematics with IC datasheets, utilizing SSH via a consumable Raspberry Pi to interface with the plug for rapid root-cause analysis.

Western Formula Racing | EV FSAE Team — London, ON
Grounded Low Voltage Co-Lead — *May 2025 – Present*

- Co-leading a 10-member GLV engineering team, conducting rigorous schematic and PCB layout reviews to maintain a >90% manufacturing success rate while mentoring junior members in core electrical principles.
- Redesigned the accumulator motherboard safety loop, implementing robust relay control circuitry, protection diodes, and isolated sensing to improve system reliability and ensure full Formula SAE compliance.
- Led the CAD and schematic design of 5+ custom PCB layouts, optimizing component placement and implementing selective eFuses and transient suppression methods to reduce GLV board failures by 50%.

Electrical Team Member — *Nov 2024 – Apr 2025*

- Engineered a comprehensive vehicle wire harness with 100+ connections, ensuring signal integrity and long-term durability under high-vibration conditions by strictly adhering to AEC-Q200 standards.
- Designed and implemented a Brake System Plausibility Device to monitor brake and throttle inputs, autonomously opening the shutdown circuit under hazardous conditions; reduced PCB size and component count by 30%.
- Sourced and integrated electromechanical components and custom PCB enclosures, optimizing for strict spatial constraints and reducing total harness weight by 10% to improve vehicle serviceability.

Undergraduate Research Fellowship | Semantic Computing for Distributed Systems — London, ON
University of Western Ontario | Awarded to top 4 ECE Summer Research Applicants — *May 2025 – Aug 2025*

- Developed an energy-efficient semantic computing framework utilizing a publish/subscribe model to optimize task-sharing and context-driven coordination across distributed computing nodes.

Projects

SoC Estimation for HV & GLV Batteries

- Designed a State of Charge estimation algorithm for both HV & LV batteries, applying Li-ion and LiPo battery theory to develop a Coulomb counting method verified through rigorous battery modeling.
- Automated cell characterization by scripting MATLAB controls for a Chroma 63600-2 DC Electronic Load, extracting parameters for a first-order equivalent circuit model with sub-10% simulation error.
- Leveraged Grafana and custom query languages to model battery thermal points, State of Health (SoH), and SoC capacity, analyzing telemetry with and without regenerative braking to justify system architecture and optimize performance.

Accumulator Motherboard & Flyback Sensing

- Engineered a modular Flyback sensing board to step down high voltage to 12V at 250mA, integrating precharge sensing circuitry to effectively decouple and protect low-voltage control systems.
- Programmed accumulator motherboard firmware with ADC integration to act as a centralized safety loop controller, dynamically managing BMS, IMD, and BSPD relays while powering Accumulator Indicator Relays (AIRs).

Low-Voltage Power Distribution Module

- Designed a custom 30 V $LiFePO_4$-powered distribution module to securely route, monitor, and protect system electronics.
- Integrated an LTC7803 synchronous step-down controller to generate a highly regulated 24 V rail, ensuring stable power delivery across fluctuating loads.
- Developed C++ firmware for the INA236 power monitoring IC, programming the MCU to actively manage power sequencing, overcurrent fault detection, and real-time CAN bus telemetry.

HV Battery Thermal Management System

- Developed a custom 1-Wire communication driver with parasitic power support to daisy-chain DS18B20 sensors, significantly reducing harness wiring by 33% while maintaining high-speed signal integrity.
- Integrated real-time thermal telemetry into the safety loop to trigger immediate shutdown during localized thermal faults, ensuring strict vehicle compliance with FSAE EV regulations.